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EXAMINER	
KANG, INSUN	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,636	KOCOT, REBECCA A.	
	Examiner	Art Unit	
	INSUN KANG	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responding to the amendment filed on 4/28/2008.

2. Claims 1 and 3-20 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 4-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Aihara (US PG Pub. 2003/0110476) in view of Stolte et al. ("Visualizing Application Behavior on Superscalar Processors," IEEE, 10/1999).

Per claim 1:

Aihara discloses:

-a sequence of instruction addresses adapted for display upon a screen that is accessible to a user (i.e. page 5, 0062; 0073);

Aihara does not explicitly teach that the screen comprises a graphical user interface (GUI) for receiving user input to select one of the instruction addresses. However, Stolte teaches a pipeline visualization system that includes a GUI for user manipulation of the pipeline instructions (i.e. page 5, left col., first paragraph). It would have been obvious for one having ordinary skill in the art to modify Aihara's disclosed system to incorporate the teachings of

Stolte. The modification would be obvious because one having ordinary skill in the art would be motivated to visualize the "state of all instructions in the pipeline at a particular cycle (page 4, 5.2 Pipeline View: Identifying problems)" and therefore allows the user to "reorder the layout of the functional units or resize the stages (page 4, right col., first paragraph)."

Aihara in view of Stolte further discloses:

-a sequence of processor pipeline stages attributable to respective ones of the instruction addresses, wherein during times when the user input is received by the GUI (i.e. page 3, 0046);

- the screen displays: a designator for at least one of the instruction addresses to denote that a corresponding designated instruction addresses will proceed to a succeeding stage in the processor pipeline during a next clock cycle; and a non-designator for another one of at least one of the instruction addresses to denote that a corresponding non-designated instruction address will not proceed to a succeeding stage in the processor pipeline during the next clock cycle (i.e. page 5, 0062; 0064; 0074).

Per claim 4:

Aihara teaches that the designator is a color that highlights the stage attributable to the at least one instruction that will proceed to the succeeding stage (i.e. page 5 lines 0064).

Per claim 5:

Aihara further discloses:

- wherein the color differs depending on which stage is highlighted (i.e. page 5 lines 0064).

Per claim 6:

Aihara further discloses:

- wherein the processor pipeline is a pipeline of a superscalar processor where more than one instruction can exist within each stage of the pipeline (i.e. page 1, 0005;page 4, 0055).

Per claim 7:

Aihara further discloses:

- wherein the user actuates a pointing device to supply the user input to the GUI for selecting only one of the instruction addresses, in response to said selection, the window displays the designator over a field bearing a stage name for all of the first instruction addresses that will proceed to the next stage in the processor pipeline (i.e. page 5, 0064).

5. Claims 8-10 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aihara (US PG Pub. 2003/0110476), in view of Beatty et al. (US Patent 5,913,052) hereafter Beatty, and further in view of Stolte et al. ("Visualizing Application Behavior on Superscalar Processors," IEEE, 10/1999).

Per claim 8:

Aihara discloses a graphics data processing system (i.e. page 5, 0062; 0073); source code represented as a first sequence of instruction addresses (i.e. page 5, 0062); a graphics rendering

engine coupled to receive the first sequence of instruction addresses and produce a graphical user interface (GUI) window (i.e. Fig. 11, the display device for the displaying module 15).

Aihara does not explicitly teach that the graphical user interface debugger includes a breakpoint field upon receiving user input via a pointing device selects a particular instruction address within the first sequence of instruction addresses shown in a particular stage of a processor pipeline. However, Beatty teaches using a breakpoint circuitry was known in the pertinent art, at the time applicant's invention was made, to allow a user to "establish at least one breakpoint for interrupting the operation of" a program (i.e. col. 3 lines 52-57). It would have been obvious for one having ordinary skill in the art to modify Aihara's disclosed debugger to incorporate the teachings of Beatty. The modification would be obvious because one having ordinary skill in the art would be motivated to "predefine pausing points, permitting the user to examine DSP states at the breakpoints (i.e. col. 3 lines 52-57)."

Aihara further discloses: displays all instruction addresses within the first sequence of instruction addresses along with corresponding stages of the processor pipeline during a clock cycle in which the particular instruction address is within the particular stage (i.e. page 3, 0046); assigns a designator to at least one instruction address of the first sequence of instruction addresses to denote that a corresponding designated instruction will proceed to a succeeding stage in the processor pipeline during a clock cycle succeeding the clock cycle (i.e. page 5, 0062; page 6, 0076); assigns a non-designator to another at least one instruction address of the first sequence of instruction addresses to denote that a corresponding non-designated instruction will not proceed to a succeeding stage in processor pipeline during a clock cycle succeeding the clock cycle (i.e. page 5, 0062; 0064; 0074).

Aihara does not explicitly teach that an instruction address field that, upon selection by a user via the pointing device, allows the user to move said another at least one instruction address. However, Stolte teaches a pipeline visualization system that includes a GUI for user manipulation of the pipeline instructions (i.e. page 5, left col., first paragraph). It would have been obvious for one having ordinary skill in the art to modify Aihara's disclosed system to incorporate the teachings of Stolte. The modification would be obvious because one having ordinary skill in the art would be motivated to visualize the "state of all instructions in the pipeline at a particular cycle (page 4, 5.2 Pipeline View: Identifying problems)" and therefore allows the user to "reorder the layout of the functional units or resize the stages (page 4, right col., first paragraph)."

Aihara and Stolte further discloses: a scheduler that responds to the moved said another at least one instruction address to form a second sequence of instructions that has a higher instruction throughput in the processor pipeline than the first sequence of instructions (i.e.Aihara, page 5, 0063; Stolte, page 6, right col., second paragraph).

Per claim 9:

Aihara further discloses:

- wherein the graphics rendering engine further displays all instructions within the first sequence of instructions and assigns a designator to a number of the instruction address of the second sequence of instructions that exceed a number of the at least one instruction address of the first sequence of instruction addresses (i.e. page 5, 0062).

Per claim 10:

Aihara further discloses:

-wherein the second sequence of instructions requires fewer clock cycles through the processor pipeline than the first sequence of instructions (i.e. page 4, 0057).

Per claims 12-15, they are the method versions of claims 4-7, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 4-7 above.

6. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aihara (US PG Pub. 2003/0110476), in view of Beatty et al. (US Patent 5,913,052) hereafter Beatty.

Per claim 16:

Aihara discloses a debugger system displaying progression of instruction addresses through a processor pipeline (i.e. page 5, 0062; 0073). Aihara does not explicitly teach that the graphical user interface debugger includes a breakpoint field for selecting a breakpoint within a breakpoint column of a display screen via user input at a breakpoint location on the display screen. However, Beatty teaches using a breakpoint circuitry was known in the pertinent art, at the time applicant's invention was made, to allow a user to "establish at least one breakpoint for interrupting the operation of" a program (i.e. col. 3 lines 52-57). It would have been obvious for one having ordinary skill in the art to modify Aihara's disclosed debugger to incorporate the teachings of Beatty. The modification would be obvious because one having ordinary skill in the art would be motivated to "predefine pausing points, permitting the user to examine DSP states at the breakpoints (i.e. col. 3 lines 52-57)."

Aihara and Beathy disclose a GUI debugging system but do not explicitly teach the breakpoint field that allows a user to select a breakpoint within a breakpoint column of a display screen to select an instruction address within the same line as the breakpoint. However, it would have been obvious at the time the invention was made to modify Aihara and Beathy's system to add a breakpoint column in the same line as the instruction address associated with a breakpoint to be hit for examination, for the purpose of visualizing the corresponding breakpoint for the instruction address in the same line, if desired.

Aihara in view of Beatty further discloses:

-a clock cycle associated with the selected instruction address being in a stage within the processor pipeline (i.e. page 3, 0046); designating all instruction addresses within the processor pipeline that will proceed to a succeeding stage of the processor pipeline; and not designating all instruction addresses within the processor pipeline that will not proceed to a succeeding stage of the processor pipeline (i.e. page 5, 0062; 0064; 0074).

Per claim 17:

Aihara further discloses:

- wherein said designating comprises receiving a signal from a stage debug register by a graphics rendering engine to denote that the instruction addresses being designated will proceed to the succeeding stage of the processor pipeline (i.e. page 5, 0074).

Per claim 18:

Aihara further discloses:

- wherein said designating comprises checking resources of a processor to determine if the instruction addresses will be allowed to proceed and, if so, sending a signal from a debug register that stores the checking outcome to designate the instruction addresses that have corresponding resources available to allow such instruction addresses to proceed (i.e. page 5, 0074).

Per claims 19 and 20, they are the method versions of claims 12 and 13, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 12 and 13 above.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aihara (US PG Pub. 2003/0110476) in view of Stolte et al. ("Visualizing Application Behavior on Superscalar Processors," IEEE, 10/1999), and further in view of Hill et al. (Pg. Pub. 2002/0130871) hereafter Hill.

Per claim 3:

Aihara and Stolte do not explicitly teach that the window comprises a pop-up window rendered upon a computer display screen. However, Hill teaches such a pop-up window was known in the pertinent art, at the time applicant's invention was made, to display additional information without using a standard window (i.e. 0102). It would have been obvious for one having ordinary skill in the art to modify the system of Aihara and Stolte to incorporate the teachings of Hill. The modification would be obvious because one having ordinary skill in the art would be motivated to display a pop-up window for additional information if desired.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aihara (US PG Pub. 2003/0110476) in view of Beatty et al. (US Patent 5,913,052) hereafter Beatty, further in view of Stolte et al. ("Visualizing Application Behavior on Superscalar Processors," IEEE, 10/1999), and still further in view of Hill et al. (Pg. Pub. 2002/0130871) hereafter Hill.

Per claim 11:

Aihara, Beatty, and Stolte do not explicitly teach that the window comprises a pop-up window rendered upon a computer display screen. However, Hill teaches such a pop-up window was known in the pertinent art, at the time applicant's invention was made, to display additional information without using a standard window (i.e. 0102). It would have been obvious for one having ordinary skill in the art to modify the system of Aihara combined with Beatty and Stolte to incorporate the teachings of Hill. The modification would be obvious because one having ordinary skill in the art would be motivated to display a pop-up window for additional information if desired.

Response to Arguments

9. Applicant's arguments with respect to claims 1 and 3-20 have been considered but are moot in view of the new ground(s) of rejection.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to INSUN KANG whose telephone number is (571)272-3724. The examiner can normally be reached on M-R 7:30-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis A. Bullock, Jr. can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Insun Kang/
Examiner, Art Unit 2193